REMARKS/ARGUMENT

Claims 12-15 are allowed. Claim 13 has been amended to delete a duplicated phrase.

Claim 16 has been amended to depend from allowed Claim 13. Accordingly, Claim 16 stands allowable.

1) Claims 5, 8 and 18 stand rejected under nonstatutory obviousness-type double patenting as being unpatentable over Claims 3 and 4 of copending Application No. 11/105,755. Applicants respectfully traverse this rejection:

In rejecting Claims 5, 8 and 18 the Examiner has not appropriately compared Claims 5, 8 and 18 of the present application with Claims 3 and 4 of copending Application No. 11/105,755. The Examiner makes the following determination:

> Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the claims is the instant application recites "a plurality of operational blocks that interconnect the adaptive equalizers" while the co-pending application recites "control logic interconnecting at least some of the adaptive equalizers". Although the terms used in the instant application and the co-pending application is different, it does not define a patentable distinct invention between the two claims since they perform the same function to interconnect the plurality of adaptive equalizer (Office Action dated March 5, 2009, page 3, lines 16-17 & page 8, lines 2-8).

Applicants respectfully submit that the Examiner has not established a prima facie case of obviousness-type double patenting for Claims 5, 8 and 18. In order to establish a prima facie case of obviousness-type double patenting, **the Examiner must establish that the claims of the present application are obvious over the CLAIMS of the cited patent**

(copending Application No. 11/105,755, now U.S. Patent No. 7,561,618). Applicants direct the Examiner's attention to MPEP § 804(B)(1):

> In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is – **does any claim in the application define an invention that is merely an obvious variation of an invention claimed in the patent**? If the answer is yes, then an "obvious-type" nonstatutory double patent rejection may be appropriate.
>
> (A) Determine the scope and content of a patent claim and the prior art relative to a claim in the application at issue;
>
> (B) Determine the **differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue**;
>
> (C) **Determine the level of ordinary skill in the pertinent art**; and
>
> (D) **Evaluate any objective indicia of nonobviousness**.
>
> The conclusion of obvious-type double patenting is made in light of these factual determinations.
>
> Any obvious-type double patent rejection should make clear:
>
> (A) The **differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application**; and
>
> (B) The **reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent**.
>
> When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, **the disclosure of the patent may not be used as prior art**. This does not mean that one is precluded from all use of the patent disclosure.

Applicants respectfully submit that the Examiner has not: (B) Determined the **differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue**; (C) **Determined the level of ordinary skill in the pertinent art**; and (D) **Evaluate any objective indicia of nonobviousness**. Moreover, Applicants respectfully submit

that the Examiner has not completely identified the **differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application**, as required by (A) above and has not provided **reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent**, as required in (B) above.

More particularly, independent Claim 5 of the present application requires and positively recites, an **apparatus**, comprising:

two or more adaptive equalizers;

a **plurality of operation blocks** that interconnect the adaptive equalizers;

a first control mechanism that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles;

a second control mechanism that disables **at least one of said plurality of operational blocks** according to the different signal delay profiles; and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different delay profiles.

In contrast, Claim 3 of copending Application No. 11/105,755, now U.S. Patent No. 7,561,618, requires and positively recites, a **system**, comprising:

a plurality of adaptive equalizers **adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate (MDPE)**;

control logic interconnecting **at least some** of the adaptive equalizers;

a first control mechanism that, according to different MDPEs, configures **at least some** of the adaptive equalizers and circuit control logic;

a second control mechanism that disables **at least a portion of said control logic** according to the different MDPEs; and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs.

The above high-lighted elements in Claim 5 of the pending application are not found in Claim 3 of U.S. Patent No. 7,561,618 and visa versa. Accordingly, the double-patenting rejection of Claim 5 over Claim 3 of U.S. Patent 7,561,618 is improper and must be reversed.

Moreover, case law requires that "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The Examiner has not considered ALL of the elements of Claim 5. As such, the Examiner has not established a prima facie case of obviousness-type double patenting for Claim 5 over Claim 3 of U.S. Patent No. 7,561,618. Moreover, Examiner has not set forth evidence satisfying all of the requirements of MPEP 804(B)(1). The rejection is improper and must be reversed.

Independent Claim 8 of the present application requires and positively recites, an **apparatus**, comprising:

two or more adaptive equalizers;

a **plurality of operation blocks** that interconnect the adaptive equalizers;

a first control mechanism that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles;

a second control mechanism that disables **at least one of said plurality of operational blocks** according to the different signal delay profiles; and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different delay profiles, the first, second, and third

control mechanisms comprise multiplexers that receive control signal according to the different delay profiles.

In contrast, Claim 4 of copending Application No. 11/105,755, now U.S. Patent No. 7,561,618, requires and positively recites, a **system**, comprising:

a plurality of adaptive equalizers **adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate** (MDPE);

control logic interconnecting **at least some** of the adaptive equalizers;

a first control mechanism that, according to different MDPEs, configures **at least some** of the adaptive equalizers and circuit control logic;

a second control mechanism that disables **at least a portion of said control logic** according to the different MDPEs; and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs, the first, second and third control mechanisms comprise multiplexers that receive control signals according to the different MDPEs.

The above high-lighted elements in Claim 8 of the pending application are not found in Claim 4 of U.S. Patent No. 7,561,618 and visa versa. Accordingly, the double-patenting rejection of Claim 8 over Claim 4 of U.S. Patent 7,561,618 is improper and must be reversed.

Moreover, case law requires that "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The Examiner has not considered ALL of the elements of Claim 8. As such, the Examiner has not established a prima facie case of obviousness-type double patenting for Claim 8 over Claim 4 of U.S. Patent No. 7,561,618.

Moreover, Examiner has not set forth evidence satisfying all of the requirements of MPEP 804(B)(1). The rejection is improper and must be reversed.

Independent Claim 18 of the present application requires and positively recites, an **apparatus**, comprising:

two or more adaptive equalizers;

a **plurality of operation blocks** that interconnect the adaptive equalizers;

a first control mechanism that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles;

a **means for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks according to the attributes of a signal profile**; and

a means for disabling a computation resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile, the means for selectively interconnecting and the means for disabling comprisinges a plurality of multiplexers.

In contrast, Claim 4 of copending Application No. 11/105,755, now U.S. Patent No. 7,561,618, requires and positively recites, a **system**, comprising:

a plurality of adaptive equalizers **adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate (MDPE)**;

control logic interconnecting at least some of the adaptive equalizers;

a first control mechanism that, according to different MDPEs, configures **at least some** of the adaptive equalizers and **circuit control logic**;

a second control mechanism that disables **at least a portion of said control logic** according to the different MDPEs; and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs, the first, second and third

control mechanisms comprise multiplexers **that receive control signals according to the different MDPEs**.

The above high-lighted elements in Claim 18 of the pending application are not found in Claim 4 of U.S. Patent No. 7,561,618 and visa versa. Accordingly, the double-patenting rejection of Claim 18 over Claim 4 of U.S. Patent 7,561,618 is improper and must be reversed.

Moreover, case law requires that "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The Examiner has not considered ALL of the elements of Claim 18. As such, the Examiner has not established a prima facie case of obviousness-type double patenting for Claim 18 over Claim 4 of U.S. Patent No. 7,561,618. Moreover, Examiner has not set forth evidence satisfying all of the requirements of MPEP 804(B)(1). The rejection is improper and must be reversed.

2) Claims 3-8, 18-19 and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597). Applicants respectfully traverse this rejection as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780,

1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification**. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious**. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Independent Claim 5 requires and positively recites, an apparatus, comprising: "two or more adaptive equalizers", "a plurality of operation blocks that interconnect the adaptive equalizers", "a first control mechanism that **configures the adaptive equalizers and the plurality of operational blocks** according to different signal delay profiles", "a second control mechanism that **disables at least one of said plurality of operational blocks** according to the different signal delay profiles" and "a third control mechanism that **disables a computation resource of at least one of said adaptive equalizers** according to the different delay profiles".

Independent Claim 8 requires and positively recites, an apparatus, comprising: "two or more adaptive equalizers", "a plurality of operation blocks that interconnect the adaptive equalizers", "a first control mechanism that **configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles**", "a second

control mechanism that **disables at least one of said plurality of operational blocks** according to the different signal delay profiles" and "a third control mechanism that **disables a computation resource of at least one of said adaptive equalizers** according to the different delay profiles, the first, second, and third control mechanisms comprise multiplexers that receive control signal according to the different delay profiles".

In contrast, Ueda discloses an apparatus that "selects" between decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or between adaptive equalizer 180 and linear adaptive equalizer 181) in response to a signal delay profile. More particularly, Ueda teaches:

> Based on the correlation value, the control signal output circuit makes a decision as to whether either one of the decision feedback adaptive equalizer 175 and the linear adaptive equalizer 176 **should be operated** with respect to its burst depending on the ratio of the value of the direct wave of the correlator to that of the delay wave thereof and the maximum delay time of the delay wave. As a criterion for this decision, there is a method of activating the linear adaptive equalizer 176 if the maximum delay time of the delay wave is less than or equal to 0.35 symbol and of activating the decision feedback adaptive equalizer 175 the maximum delay time is more than or equal to 0.35 symbol, both using the result of bit error rate performance shown in FIG. 2, for example. After the adaptive equalizer to be operated has been decided, the delay measuring circuit 174 outputs the control signal to the decision feedback adaptive equalizer 175 when the decision feedback adaptive circuit 175 is activated, whereas the delay measuring circuit 174 outputs the control signal to the linear adaptive equalizer 176 when the linear adaptive equalizer 176 is activated (col. 46, line 57 – col. 47, line 10).

In light of the above, there is selecting, but NO "configuring" of Ueda's decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or feedback adaptive equalizer 180 and linear adaptive equalizer 181), as suggested by Examiner. Accordingly, Ueda fails to teach or suggest, "a first control mechanism that **configures the adaptive equalizers and the plurality of operational blocks** according to different signal delay profiles", as required by Claims 5 and 8.

Further, while Ueda teaches that square error integrating circuit 177 selects between decision feed back adaptive equalizer 175 or linear adaptive equalizer 176 (and square error integrating circuit 182 selects between decision feed back adaptive equalizer 180 or linear adaptive equalizer 181), Examiner cites the very same mechanisms as being both the "first control mechanism" and the "third control mechanism". Examiner can not have it both ways. The same circuit in Ueda is either the "first control mechanism" or the "third control mechanism". As such, Ueda fails to teach or suggest, "a **third control mechanism** that **disables a computation resource of at least one of said adaptive equalizers** according to the different delay profiles", as required by Claims 5 and 8.

In addition to the above, Ueda teaches respective enabling of decision feed back adaptive equalizer 175 or linear adaptive equalizer 176 (and square error integrating circuit 182 selects between decision feed back adaptive equalizer 180 or linear adaptive equalizer 181), which also implies enabling of the computation resource within when an adaptive equalizer is selected. No where does Ueda teaches "disabling" of a computation resource in one of the adaptive equalizers "according to a different delay profile", as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction. Accordingly, Ueda fails to teach or suggest, "a **third control mechanism** that **disables a computation resource of at least one of said adaptive equalizers** according to the different delay profiles", as required by Claims 5 and 8.

Examiner admits that Ueda fails to teach or suggest, "a second control mechanism that **disables at least one of said plurality of operational blocks** according to the different signal delay profiles", as required by Claims 5 and 8 (OA, page 10, lines 9-10). Examiner, however, argues that this limitation would have been obvious to one of ordinary skill in the art at the time of the invention in order to deactivate the error integrated circuit of the non-selected branch as taught by the instant application in order to reduce power (OA, page 10, lines 11-18). But just because, in hindsight, it might be desirable to reduce power

consumption, one having ordinary skill in the art at the time of the invention would not necessarily been directed to reduce power consumption by disabling "at least one of the plurality of operation blocks according to different signal delay profiles", as determined by Examiner. The only reason it would be "obvious" would be after a skilled artisan reviewed the present specification. Applicants respectfully request Examiner to supply more prior art confirming that one having ordinary skill in the art would have been led to "reduce power" in the manner required by Claims 5 and 8, or withdraw the argument.

In light of the above arguments, it is clear that Ueda fails to teach or suggest ALL of the limitations of Claims 5 and 8. Accordingly, the 35 U.S.C. 103(a) rejection of Claims 5 and 8 is improper and must be withdrawn.

Applicants further object to Examiner's reliance on Sellmair (US 6,978,405 B1), as teaching a control mechanism for deactivating comprising multiplexer that receives control signal (in his rejection of Claim 8), being Sellmair is NOT cited as a reference by Examiner in any of the Notice of References Cited (PTO-892) forms and is not cited as a reference to be combined with Ueda (OA, page 8, lines 17-18). Accordingly, it is improper for Examiner to combine Sellmair with Ueda as applied to Claim 8 when the rejection of Claim 8 is a 35 U.S.C. 103(a) rejection over Ueda. Examiner should remove the reference from his comments OR officially correct the record.

Claims 3, 4, 6 and 7 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 3 further defines the apparatus of claim 5 wherein each of said two or more adaptive equalizers comprise a computational resource. Claims 3 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Claim 4 further defines the apparatus of claim 3 wherein the computation resource comprises at least one item selected from the group consisting of: a summer, a conjugation block, a multiplier, and a divider. Claims 4 stands allowable as depending from allowable Claim 3 and including further limitations not taught or suggested by the references of record.

Claim 6 further defines the apparatus of claim 5 wherein said operational blocks comprise at least one item selected from the group consisting of: "a signal regenerator", "a delay line" and "a summer". Accordingly, Claim 6 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Claim 7 further defines the apparatus of claim 5 wherein the different signal delay profiles comprise at least one multi-path signal profile selected from the group consisting of: "sub-signals that arrive to the apparatus in consecutive chip time unit", "sub-signals wherein **one sub-signal comprises a substantial amount of total energy of the sub-signals**", "sub-signals that do not arrive to the apparatus in consecutive chip time units", "sub-signals that arrive to the apparatus in **two or more clusters**" and "sub-signals that arrive to the apparatus from more than one antenna". Claims 7 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record. Moreover, Examiner cites no authority in Ueda that teaches or suggests "sub-signals wherein **one sub-signal comprises a substantial amount of total energy of the sub-signals**". Examiner is silent. Further, while Ueda teaches that when a delay wave is less than or equal to 0.35 symbol linear adaptive equalizer 176 is selected, whereas if the maximum delay time of the delay wave is more than 0.35, then decision feedback adaptive equalizer 175 is selected (col. 46, line 63 – col. 47, line 3), Ueda does not further teach or suggest any "clusters" of signals as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight

reconstruction. Accordingly, Claim 7 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Independent 18 requires and positively recites, a system comprising: "two or more adaptive equalizers", "a plurality of operational blocks", "a means for **selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks according to the attributes of a signal profile**" and "a means for **disabling a computation resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile**, the means for selectively interconnecting and the means for disabling comprising a plurality of multiplexers".

In contrast, Ueda discloses an apparatus that "selects" between decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or between adaptive equalizer 180 and linear adaptive equalizer 181) in response to a signal delay profile. More particularly, Ueda teaches:

> Based on the correlation value, the control signal output circuit makes a decision as to whether either one of the decision feedback adaptive equalizer 175 and the linear adaptive equalizer 176 **should be operated** with respect to its burst depending on the ratio of the value of the direct wave of the correlator to that of the delay wave thereof and the maximum delay time of the delay wave. As a criterion for this decision, there is a method of activating the linear adaptive equalizer 176 if the maximum delay time of the delay wave is less than or equal to 0.35 symbol and of activating the decision feedback adaptive equalizer 175 the maximum delay time is more than or equal to 0.35 symbol, both using the result of bit error rate performance shown in FIG. 2, for example. After the adaptive equalizer to be operated has been decided, the delay measuring circuit 174 outputs the control signal to the decision feedback adaptive equalizer 175 when the decision feedback adaptive circuit 175 is activated, whereas the delay measuring circuit 174 outputs the control signal to the linear adaptive equalizer 176 when the linear adaptive equalizer 176 is activated (col. 46, line 57 – col. 47, line 10).

In light of the above, there is selecting, but NO "selective interconnecting" of decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or feedback adaptive equalizer 180 and linear adaptive equalizer 181), much less any "selective interconnecting of decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 (or feedback adaptive equalizer 180 and linear adaptive equalizer 181) with square error integrating circuits 177 & 182, as determined by Examiner. As such, Ueda fails to teach or suggest, "**selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks according to the attributes of a signal profile**", as required by Claim 18.

In addition to the above, Ueda teaches respective enabling of decision feed back adaptive equalizer 175 or linear adaptive equalizer 176 (and square error integrating circuit 182 selects between decision feed back adaptive equalizer 180 or linear adaptive equalizer 181), which also implies enabling of the computation resource within when an adaptive equalizer is selected. No where does Ueda teaches "disabling" of a computation resource in one of the adaptive equalizers "according to a different delay profile", as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction. Accordingly, Ueda fails to teach or suggest, "a means for **disabling a computation resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile,** the means for selectively interconnecting and the means for disabling comprising a plurality of multiplexers", as further required by Claim 18.

Examiner admits that Ueda fails to teach or suggest, "deactivating according to different delay profile and that the disabling mechanism comprises multiplexers that receive control signals", as required by Claim 18 (OA, page 16, lines 5-7). Examiner, however, argues that this limitation is taught by Sellmair (US 6,978,405 B1) (OA, page 16, lines 7-10).

Applicants object to Examiner's reliance on Sellmair (US 6,978,405 B1), as teaching a control mechanism for deactivating comprising multiplexer that receives control signal (in his rejection of Claim 18), being Sellmair is NOT cited as a reference by Examiner in any of the Notice of References Cited (PTO-892) forms and is not cited as a reference to be combined with Ueda (OA, page 8, lines 17-18). Accordingly, it is improper for Examiner to combine Sellmair with Ueda as applied to Claim 18 when the rejection of Claim 18 is a 35 U.S.C. 103(a) rejection over Ueda. Examiner should remove the reference from his comments OR officially correct the record.

But even if Examiner corrects the record and adds Sellmair to Ueda in a future 35 U.S.C. 103(a) rejection, Sellmair does not teach or suggest the above identified deficiencies of Ueda as applied to Claim 18. As a result, any purported combination of Ueda and Sellmair fails to teach or suggest all of the limitations of Claim 18. In light of the above arguments, it is clear that Ueda, alone or in combination with Sellmair, fails to teach or suggest ALL of the limitations of Claim 18. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 18 is improper and must be withdrawn.

Claims 19 and 22 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 3 further defines the apparatus of claim 5 wherein each of said two or more adaptive equalizers comprise a computational resource. Claims 3 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record.

Claim 19 further defines the system of claim 18 further comprising means for disabling at least one of the plurality of operational blocks according to said attributes of

the signal profile. Claims 19 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record.

Claim 22 further defines the system of claim 18, wherein the attributes of the signal profile comprise at least one selected from the group consisting of: "a number of antennas that transmitted the multi-path signal", "a length of the multi-path signal profile", "an **amount of energy in a single sub-signal of the multi-path signal**", "**an amount of capturable energy by a number of adaptive equalizers**" and "a **number of energy clusters**". Claims 22 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record. Moreover, Examiner cites no authority in Ueda that teaches or suggests, "an **amount of energy in a single sub-signal of the multi-path signal**", "**an amount of capturable energy by a number of adaptive equalizers**" and "a **number of energy clusters**". Examiner is silent. Further, while Ueda teaches that when a delay wave is less than or equal to 0.35 symbol linear adaptive equalizer 176 is selected, whereas if the maximum delay time of the delay wave is more than 0.35, then decision feedback adaptive equalizer 175 is selected (col. 46, line 63 – col. 47, line 3), Ueda does not further teach or suggest any "amount of energy in any single sub-signal of the multi-path signal" or "an amount of capturable energy by any of the equalizers", or "number of energy clusters" as determined by Examiner. Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction. Accordingly, Claim 22 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record.

3) Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Yang. Applicants respectfully traverse this rejection as set forth below.

Claim 9 further defines the apparatus of claim 5 wherein a two-stage configuration of the apparatus comprises a default mode. Claim 9 stands allowable as depending from allowable Claim 5 and including further limitations not taught or suggested by the references of record. Moreover, even if, arguendo, Yang discloses wherein a two-stage configuration of the apparatus comprises a default mode, as suggested by Examiner, Yang fails to teach or suggest the above identified deficiencies of Ueda as applied to Claim 5. Accordingly, any combination of Ueda and Yang fails to teach or suggest all of the limitations of Claim 9, as is required by law. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 9 is improper and must be withdrawn.

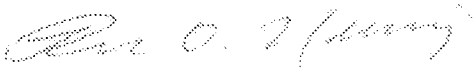
4) Claim 21 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) as applied to claim 18 above, and further in view of Juan (US 5,642,382). Applicants respectfully traverse this rejection as set forth below.

Claim 21 further defines the system of Claim 18 by further comprising means for sharing computational resources of the two or more adaptive equalizers. Claim 21 stands allowable as depending from allowable Claim 18 and including further limitations not taught or suggested by the references of record. Moreover, even if, arguendo, Juan discloses a system that shares a single set of arithmetic operators between filters of the equalizers, as suggested by Examiner, Juan fails to teach or suggest the above identified deficiencies of Ueda as applied to Claim 18. Accordingly, any combination of Ueda and Juan fails to teach or suggest all of the limitations of Claim 21, as is required by law. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 21 is improper and must be withdrawn.

Claims 12-15 are allowed. Objected to Claim 16 has been amended to be allowable. Claims 3-9, 11, 18, 19 and 21 are allowable over the cited art for the reasons

set forth above. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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